Amendments of the Specification

Please amend the Abstract, on page 37 of the specification, as shown in the following amended version of the Abstract:

[0071] A multiplier-accumulator (MAC) block can be programmed to operate in one or more modes. When the MAC block implements at least one multiply-and-accumulate operation, the accumulator value can be zeroed without introducing clock latency or initialized in one clock cycle. To zero the accumulator value, the most significant bits (MSBs) of data representing zero can be input to the MAC block and sent directly to the add-subtract-accumulate unit. Alternatively, dedicated configuration bits can be set to clear the contents of a pipeline register for input to the add-subtract-accumulate unit. ~~The least significant bits (LSBs) can be tied to ground and sent along the feedback path. To initialize the accumulator value, the MSBs of the initialization value can be input to the MAC block and sent directly to the add-subtract-accumulate unit. The LSBs can be sent to another multiplier that performs a multiply-by-one operation before being sent to the add-subtract-accumulate unit.~~